Technical Progress Report 05/01/93 – 08/01/93
Construction of a Connectionist Network Supercomputer
University of California, Berkeley
ONR URI Grant No. N00014-92-J-1617

1 Introduction

This quarter we focused our attention on the completion of the hardware and software implementations for the T0 processor. The T0 design represents a significant step towards the development of the T1 processor for the CNS-1 machine. T0 is essentially a uniprocessor version of the T1 multiprocessor node. We also began detailed investigations into the design of the Rambus high-speed memory interface for the T1 processor and began a study on the CNS-1 input/output processor, Hydrant. This quarter we have also reached an important milestone in our research on analog VLSI preprocessors for the CNS-1 machine.

The CNS-1 project continues to have a significant effect on the education of graduate and undergraduate students at our institution. There are currently 11 Ph.D., 2 M.S., and 2 B.S. students associated with the project.

2 Technical Status

2.1 T0 Design

The core VLSI design team has continued work on the implemention the first Torrent processor, T0. The T0 chip is a major design effort and rivals industrial microprocessors in size and complexity. It is a significant step towards the design of the T1 processor to be used in the CNS-1 machines. It is implementated as a mixture of full custom and standard cells in a 1.2μm CMOS process. Significant progress has been made this quarter. Most of the layout for the custom datapaths for has been designed and verified. Currently we are specificating and automatically synthesizing of the processor controller, and completing chip integration and verification. The fabrication deadline for the chip has been moved to next quarter.

The T0 software emphasis has been on producing code to aid T0 hardware verification. A Torrent assembler has been finished and tested, as has an Instruction Set Architecture (ISA) simulator for the T0 processor. The ISA simulator now includes modifications to support a more accurate machine model and better facilities for multi-processor simulations. This will allow full testing of hardware-dependent system software for T0 without using the slower register-transfer-level simulator, and will provide similar facilities for T1. Several thousand lines of assembler test code have been produced, and these have been used to verify the vector unit on the Torrent simulators, and also to debug development tools.

The specification for an operating system kernel and host server program for T0 has been written, and initial development is underway—migration paths to CNS-1 system software have been a major consideration in this process. Finally, work has continued on Torrent library routines—again, the emphasis is on producing a variety of routines to test the T0 hardware simulations.

2.2 Software

Considerable progress was made on all levels of the software for the CNS-1 project. The entire suite of system support software for exercising a single Torrent chip was designed and largely complete. A new and more general package for handling large complex data sets was released to users. At a higher level, the BoB package for describing layered networks was designed and a preliminary version made available for experimental use. The pSather project on general purpose parallel programming also made several significant advances. The design was completed and a Technical Report describing the design rationale was written; shorter versions have been presented at local and international meetings. A variety of ambitious applications have been coded for the CM-5 and provided insights into design issues.

A major effort of this period was a summer study on mapping key applications to the CNS-1 architecture. The applications considered include vision, speech, language processing, and semantic networks as well as the benchmark problems in neural networks. This has already led to some design changes in the T1 chip architecture and raised a number of issues for further study. We expect at least one journal paper to result from these studies. The summer studies were done by graduate students, and helped introduce them to the CNS-1 project.

2.3 Analog VLSI preprocessors

In this quarter, an important milestone was reached in our research on analog VLSI preprocessors for auditory applications. An analog VLSI model of auditory spectral shape processing returned from fabrication, and initial tests show it is functioning properly. The 34,000 transistor transistor chip processes an analog auditory input, producing a 119 channel spectral representation. The chip output is in digital format; we are using this chip as a peripheral input device to a Sun workstation. Our next task is to begin experiments to test the performance of the device as a front end for speech recognition and other applications.

Several unique technologies were developed for the interface aspects of this device. A new communications protocol, the address-event representation, was developed for efficient data transfer between the chip and the host computer; this research was in collaboration with researchers at Caltech, Oxford, Tanner Inc. and Synaptics Inc. The parameters that control the analog circuits are stored on-chip using floating-gate technology, and programmed under digital control using a novel tunneling circuit; this technology was developed in collaboration with Alan Kramer of UC Berkeley.

3 Publications and Talks

This section lists the recent publications and talks.

Appeared:

Asanović, K., Morgan, N., and Wawrzynek, J., "Using Simulations of Reduced Precision Arithmetic to Design a Neuro-Microprocessor," *Journal of VLSI Signal Processing*, 6, pages 33–44, June 1993.

Wawrzynek, J., Asanović, K., and Morgan, N., "The Design of a Neuro-Microprocessor," IEEE Transactions on Neural Networks, May 1993.

Lazzaro, J., Wawrzynek, J., Mahowald, M., Sivilotti, M., and Gillespie, D. (1993). "Silicon auditory processors as computer peripherals," in *Advances in Neural Information Processing Systems 5*, San Mateo, CA: Morgan Kaufmann Publishers. A longer version appeared in *IEEE Transactions on Neural Networks*, May 1993.

To Appear:

Asanović, K.,Beck, J., Feldman, J., Morgan, N., and Wawrzynek, J., "Designing a Connectionist Network Supercomputer," *International Journal on Neural Systems*, Fall 1993.

4 Colloquia and invited lectures

Lazzaro, J., "Energy, Wires, Neurons, and Analog VLSI," invited talk at *Neural Networks for Physics III*, Theoretical Physics Institute, University of Minnesota, July 14-17, 1993.

Wawrzynek, J., "Development of a Connectionist Network Supercomputer," AT&T Bell Laboratories, Holmdel, NJ, June 11, 1993.

Wawrzynek, J., "Development of a Connectionist Network Supercomputer," Department of Computer Science and Engineering, University of Washington, Seattle, Washington, June 2, 1993.

Lazzaro, J., "Analog VLSI and Silicon Audition," colloquium talk, The Moore School of Electrical Engineering, The University of Pennsylvania, May 1993,